LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A process for forming a housing for electronic modules, comprising the steps of:

providing a substrate having one or more regions, the one or more regions having a structure selected from the group consisting of semiconductor structures, connection structures, structures for forming semiconductor structures, and structures for forming connection structures, the substrate having at least a first substrate side to be encapsulated and an underside;

providing a vapor-deposition glass source;

arranging the first substrate side in such a manner with respect to the vapor-deposition glass source that the first substrate side can be vapor-coated;

vapor-coating the first substrate side with a glass layer ;

thinning the substrate on the underside;

using the structure as an etching stop while producing etching pits on the underside so that the etching pits extend through the substrate to the structure; and

producing line contacts on the underside.

2. (Previously presented) The process as claimed in claim 1, wherein the one or more regions are arranged on the first substrate side.

3. (Previously presented) The process as claimed in claim 2, further comprising providing the substrate with a passivation layer on a second side that is on the opposite side from the first substrate side.

4. (Previously presented) The process as claimed in claim 1, wherein the substrate comprises a wafer, the process further comprising packaging of components which still form part of the wafer.

5. (Previously presented) The process as claimed in claim 1, further comprising vapor-coating a second substrate side with a glass layer.

6. (Previously presented) The process as claimed in claim 1, wherein the vapor-deposition glass source generates at least a binary glass system.

7. (Previously presented) The process as claimed claim 1, wherein the first substrate side is vapor-coated until the glass layer has a thickness in the range from 0.01 to 1000 μm on the first substrate side.

8. (Previously presented) The process as claimed in claim 1, wherein the step of providing the vapor-deposition glass source comprises providing a reservoir having organic constituents, and converting the organic constituents into the vapor state through application of a vacuum or through heating so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the first substrate side.

9. (Previously presented) The process as claimed in claim 1, wherein the glass layer has a thickness in the range between 0.1 and 50 μm.

10. (Previously presented) The process as claimed claim 1, wherein the glass layer has a thickness in the range between 50 and 200 μm.

11. (Previously presented) The process as claimed in claim 1, wherein vapor-coating the first substrate side with the glass layer comprises generating a vapor from a glass target by means of an electron beam.

12. (Previously presented) The process as claimed in claim 11, wherein the glass target is a borosilicate glass comprising aluminum oxide and alkali metal oxide fractions.

13. (Previously presented) The process as claimed in claim 1, wherein the glass layer has a coefficient of thermal expansion that is virtually equal to that of the substrate.

14. (Previously presented) The process as claimed in claim 1, wherein the glass layer provides a hermetic seal.

15. (Previously presented) The process as claimed in claim 1, further comprising vapor deposting a plurality of glass layers onto the substrate.

16. (Previously presented) The process as claimed in claim 1, further comprising removing material from a second substrate side, the second substrate side being on the opposite side from the first substrate side.

17. (Previously presented) The process as claimed in claim 1, wherein the substrate includes a wafer having a plurality of the structures wherein the process further comprises dividing the wafer to form a plurality of electronic modules which each have first encapsulated sides.

18. (Previously presented) The process as claimed in claim 38, further comprising providing the underside with a plastic covering without providing the ball grid array with the plastic covering.

19. (Previously presented) The process as claimed in claim 39, further comprising vapor coating the underside with the glass layer after the plastic layers have been removed from the underside and dividing up the wafer so that the plurality of electronic modules are encapsulated on both sides.

20. (Previously presented) The process as claimed in claim 19, wherein the glass layer on the underside has a thickness in the range from 1 to 50 μm.

21. (Previously presented) The process as claimed in claim 36, further comprising filling in the etching pits with conductive material.

22. (Previously presented) The process as claimed in claim 1, wherein vapor-coating the first substrate side with the glass layer comprises plasma ion assisted deposition.

23. (Currently amended) An electronic module, comprising:

a substrate having a first substrate side and a second substrate side opposite the first substrate side;

one or more semiconductor structures and/or connection structures being disposed on the first substrate side;

a glass layer being vapor deposited on the first substrate side; and

a plurality of etched pits and line contacts being defined in the second substrate side, the plurality of etched pits extending through the substrate and stopping at the one or more semiconductor structures and/or connection structures.

24. (Previously presented) The electronic module as claimed in claim 23, further comprising a second glass layer being vapor deposited on the second substrate side.

25. (Currently amended) An electronic module, comprising:

a substrate having a first substrate side and a second substrate side opposite the first substrate side;

one or more semiconductor structures and/or connection structures being disposed on the first substrate side;

a glass layer being deposited on the first substrate side;

a plastic layer on a surface of the glass layer opposite the substrate; and

a plurality of etched pits and line contacts being defined in the second substrate side, the plurality of etched pits extending through the substrate and stopping at the one or more semiconductor structures and/or connection structures.

26. (Previously presented) The electronic module as claimed in claim 23, wherein the second substrate side is thinned after the glass layer is deposited on the first substrate side.

27. (Previously presented) The electronic module as claimed in claim 23, further comprising a passivation layer on the second substrate side.

28. (Previously presented) The electronic module as claimed in claim 23, wherein the glass layer comprises a mixed layer of inorganic and organic constituents.

29. (Previously presented) The electronic module as claimed in claim 23, wherein the glass layer comprises a plurality of glass layers.

30. (Previously presented) The electronic module as claimed in claim 29, wherein the individual layers of the plurality of glass layers have different compositions.

31. (Previously presented) The electronic module as claimed in claim 23, further comprising line contacts that are connected to the one or more semiconductor structures and/or connection structures on the first substrate side.

32. (Previously presented) The electronic module as claimed in claim 31, further comprising a ball grid array at the line contacts.

33. (Cancelled)

34. (Previously presented) The process as claimed in claim 1, further comprising applying a layer of plastic above the glass layer.

35. (Previously presented) The process as claimed in claim 15, wherein the plurality of glass layers have the same or various glass compositions.

36. (Previously presented) The process as claimed in claim 17, wherein the etching pits are produced on the underside opposite the structure.

37. (Previously presented) The process as claimed in claim 17, wherein the line contacts are produced on the underside opposite the structure.

38. (Previously presented) The process as claimed in claim 17, further comprising applying a ball grid array at the line contacts.

39. (Previously presented) The process as claimed in claim 17, further comprising lithographing plastic layers on the substrate and removing the plastic layers from the underside.

40. (Previously presented) The process as claimed in claim 39, further comprising uncovering the line contacts by local elimination of the glass layer.